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HIGHER DIMENSIONAL CORE ARRAYS
FOR MACHINE MEMORIES

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SUMMARY

This report describes a cubical memory array of magnetic cores and discusses some of the advantages and problems of higher (than two) dimensional core memory arrays.

HIGHER DIMENSIONAL CORE ARRAYS FOR MACHINE MEMORIES

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The basic advantage of the magnetic core memory systems as now used or planned for use in several large fast digital machines is that the number of electron tubes required per bit is small and that these are simple ordinary tubes easily replaced when necessary. If a square array has n^2 cores it has 2n different paths for current to pass through in exciting it. This is $2\sqrt{N}$ with N being the total bits, n^2.

We describe here a three dimensional array which can be constructed from cores identical to those used in two dimensional arrays. It has $4\sqrt[3]{N}$ paths for current to pass through. This number is indicative of the number of electron tubes needed for N bits.

Consider a simple cubical array of cores. Suppose, for example, that it has 64^3 cores. A square array to contain this many cores would be a $(512)^2$ array. The cubical would need 256 paths; the square would need 1024. As size increases clearly the relative advantage of the cubical improves.

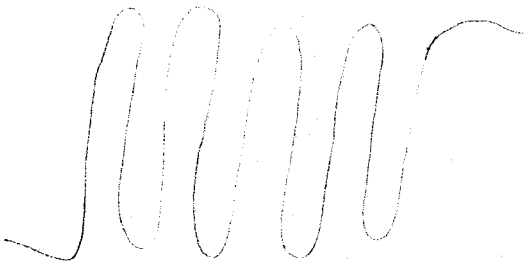
But we must show how to set up the cubical array. Let i,j,k be the three coordinates of the cores, regarded as numbers modulo 64 specifically, 0,1,2,,..,63. Then let

$$\ell = i + j + k \quad \text{modulo } 64.$$

We define the paths such that for each particular value of i one path passes through all cores with this value for the coordinate i, similarly for j and k and for ℓ. This makes four sets of paths.

The wires corresponding to the paths must pass through the cores in the same direction. That is, if the wires are oriented by the direction in which current will flow through them then all four wires which pass through a given core must pass through it in the same direction. For the first three wires or paths to pass through a core, corresponding to the values of i, or j, and of k this can be accomplished by tilting the cores properly. Thus, these paths need only be arranged to cover the required set of cores.

For example, the cores with a given valve of i lie in a plane. To cover these we can use a path of the form



Thus, the i,j, and k paths can be put in with a minimal length of wire. Having arranged this then the ℓ = const. paths will require more wire. I do not know what way is the best to arrange these. There is no particular problem

involved, especially if one accepts paths that do not run straight through the array but makes alternating detours either to avoid or to pass through in the correct direction those cores which are not turned properly for direct pass through.

An ℓ path will generally lie along 3 planes which slice diagonally through the array; these will correspond to (in the $(64)^3$ array):

$$i + j + k = \ell$$

$$i + j + k = \ell + 64$$

$$i + j + k = \ell + 128,$$

If $\ell = 63$ or $\ell = 62$ there are only two planes that meet the array.

Each ℓ path has the same number of cores, $(64)^2$, through which it must pass. The basic point of the fourth set of paths is that when core 'c is on paths i,j,k, any other core c' can be on at most two of these paths. To see this, note that for two different cores if we don't have two indices differing in the two sets i,j,k and i',j',k', in which case the assertion is certainly true, then we will have ℓ and ℓ' different as well as one pair from the other three, as i and i' or j and j' or k and k'. So, in any case the two cores can have at most two paths in common.

Now suppose that we want to flip over the magnetization of a core. We send currents through the four paths that pass through the core and we make the size of each current

half what it would be in the planar array. Since the core we want to flip has four currents passing through it, this is the same total current as that used to flip the planar array, so any other core is not flipped. This shows that the arrangement provides a mechanism for selectively flipping the magnetization of specific cores. Aside from this, to have an effective memory system, we must have a way of detecting the flipping of a core's magnetization, This brings up questions of noise and wiring for a pick-up wire (or wires). Furthermore, we need a good way to effectuate the activation of the appropriate paths in response to orders in the form of a binary digit sequence from control.

First, let us consider the problem of activating circuits. We can assume that the description of the core to be affected comes in the form of its three coordinates i,j,k, expressed as a binary sequence such as

$$\underset{i}{\underline{110101}}\ \underset{j}{\underline{010010}}\ \underset{k}{\underline{110011}} \quad .$$

The i,j, and k paths can be activated in exactly the same manner as in a planar array. For the ℓ paths we must (in effect) compute i + j + k mod 64. This is rather easy in the binary system. We need only add i,j, and k and drop all digits beyond the sixth:

$$\begin{array}{rr} i & 110101 \\ j & 010010 \\ k & \underline{110011} \\ \text{sum} & \underline{1111010} \\ \ell & 111010 \end{array}$$

This addition can be accomplished easily by a number of tubes small in comparison with the number required for gating the currents through the paths.

The noise aspect of the problem of detecting flip-over is a part of the problem which the writer is less competent to treat. But a few things may be said. One point is that the currents in the four paths used to flip a core can be turned on at different times so that only the noise effect of the last two paths will interfere with detection of a flip or non-flip. Then, the arrangement of pick-up wires can be made in consideration of this. For example, if the i and j paths involved are activated last, then a pick-up wire might work satisfactorily running along parallel to the k paths, with proper orientations.

For sufficiently large arrays, one will have to abandon the simple single pick-up wire traversing all the c cores and use a set of wires which pass through devices which respond only to a signal of sufficient strength. The output of these devices would then be simply added. This amounts to a noise filtering system. If done with tubes, the number needed would probably be somewhat less than the number needed to control one set of paths.

Other designs for higher dimensional memories can be devised which have less geometrical character. The basic principle employed above of redundant indexing has fairly direct generalizations to dimensions of any order. One

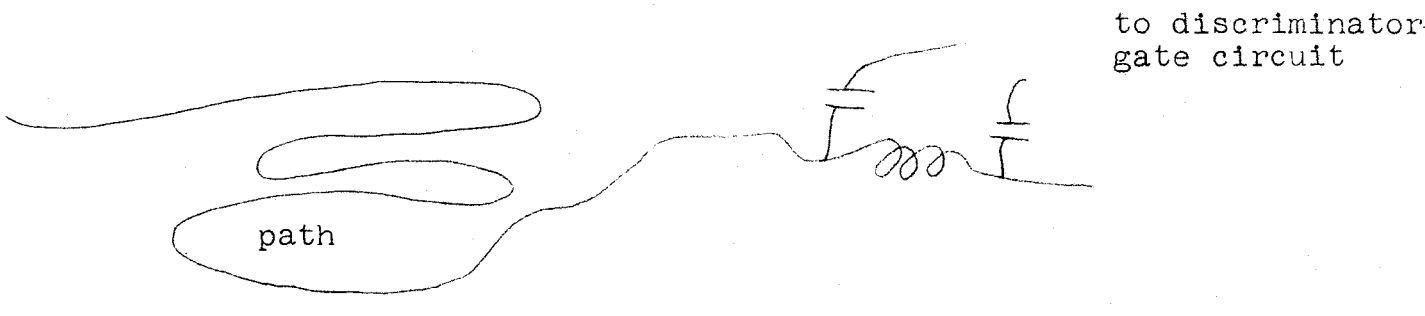
could consider arrays which have only two cores on an edge but a very high dimensionality. None of these, of course, can have as simple a geometrical form, when laid out by necessity in three dimensions, as the cubical array described.

The writer wants to give thanks and credit for valuable suggestions from A. Gleason and Willis Ware.

Appendix

It may be practical to eliminate the use of any specific pick-up wire or path in the array when we go to an array with a large number of cores and especially if it is contemplated to use a family of separate pick-up paths in order to cut down the noise factor.

Suppose we have a three dimensional array as described above, controlled by four families of current paths. And suppose we activate or flip a core by first turning on two of the currents running through two of the paths through it and then turning on the remaining two after these currents are stabilized. What we can do is to use one of the first two paths also as a pick-up path, since the major current flowing through it will be stabilized by the time the pulse given out by a flipping core will be picked up by it. This pulse can be discriminated from the steady current by an appropriate inductive or capacitative coupling to the circuit which discriminates a significant pulse from noise.

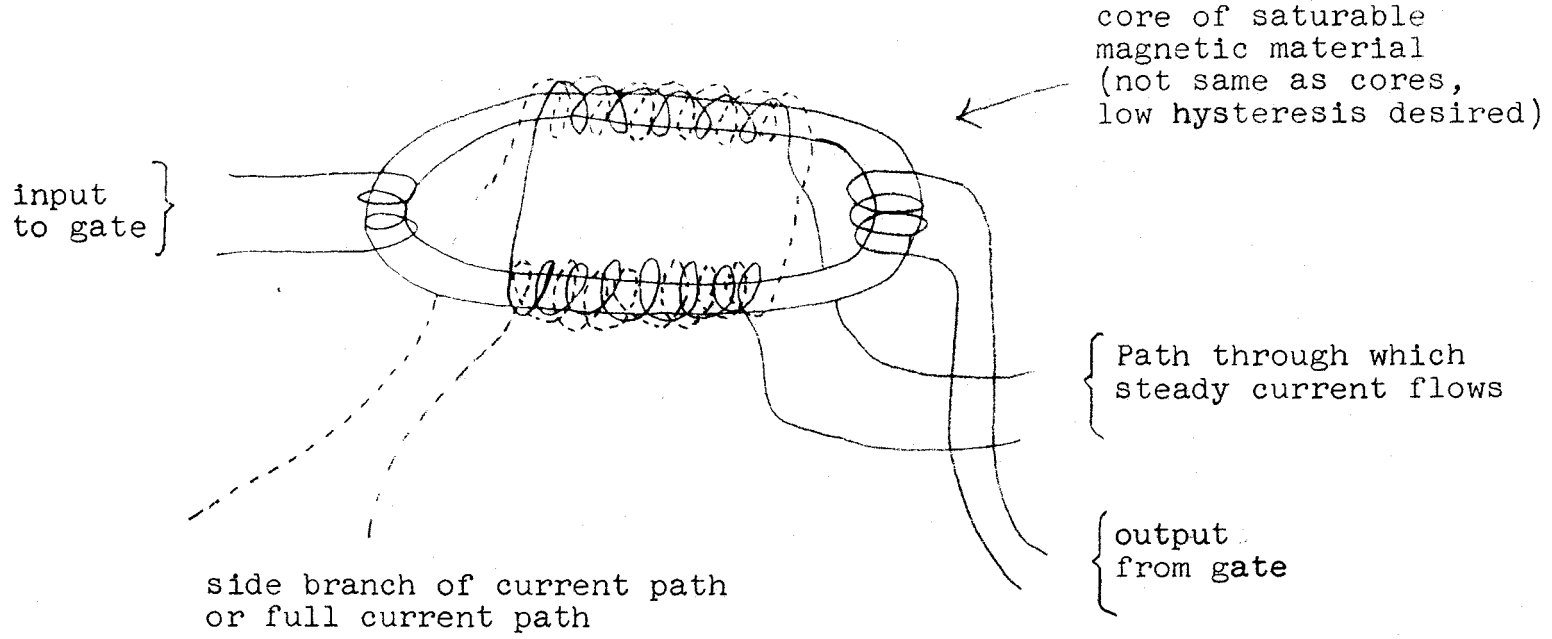


It will be easy to arrange for the discriminator circuit to be insensitive (for example, by a temporary negative grid bias) at the time the current through the path is being turned on, or to arrange that its response then should be ignored. It should also be fixed to respond only when current flows in the path.

Now consider a 64x64x64 array. Using this arrangement each pick-up path would cover 64x64 cores, no more than is covered at present so that the noise considerations would be as good as at present on a 64x64 square array.

Also, the discriminator circuits on the pick-up paths require a number of tubes probably less than for one family of current paths so this should not be too much of a burden.

The following sort of device might be appropriate for the discriminator-gate circuit associated with the pick-up path as a means of eliminating any need for tubes. It is analogous to a magnetic amplifier circuit.



The mechanism is that when current is flowing through the current path some or all of this passes through the two windings on the illustrated device and neutralizes an equal current flowing in another pair of windings so as to give an opposite effect. When current does not flow through this (broken line) the magnetic core is saturated and unresponsive to the winding connected with the input. When it does the core is demagnetized and the input is able to get through and affect the output winding.

In a 64x64x64 array, 64 of these magnetic gates would have their outputs all connected together and sent to a discriminator.

This magnetic gating would eliminate any need for any additional tubes for the individual pick-up paths.